AMENDMENT TRANSMITTAL LETTER (Large Entity) Applicant(s): **Ken Ogura**			Docket No. **OKI.244**
Serial No. **09/883,363**	Filing Date **June 19, 2001**	Examiner **H. Nguyen**	Group Art Unit **2812**

Invention: **CONDUCTOR POSTS, CONSTRUCTION FOR AND METHOD OF FABRICATING SEMICONDUCTOR INTEGRATED CIRCUIT CHIPS USING THE CONDUCTOR POST, AND METHOD OF PROBING SEMICONDUCTOR INTEGRATED CIRCUIT CHIPS**

TO THE ASSISTANT COMMISSIONER FOR PATENTS:

Transmitted herewith is an amendment in the above-identified application.

The fee has been calculated and is transmitted as shown below.

CLAIMS AS AMENDED

	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST # PREV. PAID FOR		NUMBER EXTRA CLAIMS PRESENT	RATE	ADDITIONAL FEE
TOTAL CLAIMS	13	-	24	=	0	x $18.00	$0.00
INDEP. CLAIMS	2	-	5	=	0	x $84.00	$0.00
Multiple Dependent Claims (check if applicable) ☐							$0.00
TOTAL ADDITIONAL FEE FOR THIS AMENDMENT							$0.00

☒ No additional fee is required for amendment.

☐ Please charge Deposit Account No. in the amount of
A duplicate copy of this sheet is enclosed.

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- ☒ Any additional filing fees required under 37 C.F.R. 1.16.
- ☒ Any patent application processing fees under 37 CFR 1.17.

Signature

Dated: **December 30, 2002**

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I certify that this document and fee is being deposited on with the U.S. Postal Service as first class mail under 37 C.F.R. 1.8 and is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

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OKI.244

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT APPLICATION of

Ken Ogura

Group Art Unit: 2812

Serial No.: 09/883,363

Examiner: H. Nguyen

Filed: June 19, 2001

For: CONDUCTOR POSTS, CONSTRUCTION FOR AND METHOD OF FABRICATING SEMICONDUCTOR INTEGRATED CIRCUIT CHIPS USING THE CONDUCTOR POST, AND METHOD OF PROBING SEMICONDUCTOR INTEGRATED CIRCUIT CHIPS

AMENDMENT

Honorable Assistant Commissioner for Patents
Washington, D.C. 20231

Date: December 30, 2002

Sir:

In response to the Office Action dated September 30, 2002, the following amendments and remarks are respectfully submitted in connection with the above-identified application.

In the Specification:

Replace the paragraph beginning on page 29 line 14 with the following paragraph:

B1

An electrode pad 14, a first insulating layer 12, a first photosensitive material layer 60, and a seal member layer 64A are formed on an IC chip 10 shown in FIG. 24A in the same manner as the IC chip 10 of the first embodiment of the invention (See FIG. 1E). Then, as shown in FIG. 24B, the second photosensitive material layer 62 is